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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,747	07/28/2003	Ka-Hing Fung	TSM02-0985	4863

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,747	FUNG ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *21-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's election filed on August 31, 2004. Claims 1-25 are pending, in which claims 21-25 are non-elected, without traverse.

*** The title of the invention is objected to as the word "improved" is included in part of the title, see MPEP 606. A new title is required.

Election/Restrictions

1. Claims 21-25 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in Paper mail date August 31, 2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-6,11-16,20 are rejected under 35 U.S.C. 102(e)/(a) as being anticipated by Sambonsugi et al (2003/0098486).

Re claim 1, Sambonsugi et al. teach (at Figs 1A-1O; paragraphs 30-50) a method for forming a semiconductor device comprising at least the steps of: forming a gate oxide 5 (5N,5P) over a substrate 1 and a gate electrode 6 (6N,6P, Fig 1A, paragraphs 30-31) over the gate oxide; implanting impurities into the substrate using the gate electrode as an implant mask to form a lightly-doped region 8 in the substrate (Figs 1B-1C; paragraphs 32-35; depositing second spacer material 16 adjacent the gate electrode 6 (Figs 1D-1E; paragraphs 36-37);

forming a first spacer 17a,b on the second spacer material 16 (Figs 1F); implanting impurities into the substrate and through a portion of the lightly-doped region using the first spacer 17a,b as an implant mask to form a first junction region 20,24 in the substrate (Figs 1G-1H); removing the first spacer (Figs 1H-1I; paragraphs 39-40); etching the second spacer material 16,26 to form a second spacer 16,26 adjacent the gate electrode 6 (Figs 1J-1K; paragraphs 40-42); and implanting impurities into the substrate using the second spacer 16/26 as an implant mask to form a second junction region 31 in the substrate (paragraphs 44-45). Re further independent claim 11, as similarly applied to claim 1, Sambonsugi also teaches forming the gate electrode having a gate width in a range of 40-100nm (.04-.10 micron; Fig 1A, paragraph 30), which is less than 0.13 micron as recited in claim 11, wherein the channel length beneath the gate oxide 5 is extending between the lightly doped regions 8, and thus having a channel length less than 0.04-0.10 micron of gate length (Fig 1B, paragraphs 30-33), which is less than 0.13 micron as recited in claim 11; forming a bottom layer 16 (the second spacer material as in claim 1) over the gate electrode 6 and the substrate and an upper layer 17 over the bottom layer 16, and removing portions of the upper layer 17 to form a first spacer 17a,b (Figs 1D-1F; paragraphs 36-37); and etching to remove portions of the bottom layer 16,26 to form a second spacer 16/26, and implanting impurities to form the second junction region 31 (Figs 1J-1L; paragraphs 41-45). Re claims 2 and 12, the method further includes depositing additional second spacer material 26 (or an additional bottom layer material as recited in claim 11) on the initially deposited second spacer material 16 (or an initially deposited bottom layer as recited in claim 11) prior to etching the second spacer material 16 (or the bottom layer) (Figs 1J-1K, paragraphs 41-44). Re claims 3 and 13, wherein the first junction region 20/24 is a deep junction region and the second junction region 31 is a source/drain region (Figs 1L-1M, paragraphs 44-45,38-39). Re claims 4 and 14, wherein the first spacer 17a,b comprises an oxide (paragraphs 37,41; or an upper layer 17 of oxide as recited in claim 14), and the second spacer 16,26 material comprises a nitride (Figs 1E-1K, paragraphs 37,41; or the bottom layer 16,26 of nitride as recited in claim 14). Re claims 5 and 15, wherein the second spacer 26,16 has a width less than a width of the first spacer 17 (Figs 1F,1K; paragraphs 37,41; by removing portions of the bottom layer 26,16 to form the second spacer,26,16). Re claims 6 and 16, wherein the method includes forming a silicide 33 over the source/drain region 31 (Figs 1O; paragraph 47).

Re claim 20, wherein the method includes forming a liner layer 15 on the gate electrode 6 and the substrate prior to depositing the bottom layer 16 (Fig 1D; paragraphs 36-37).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 7,17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sambonsugi et al (2003/0098486) taken with Yamaguchi et al (5,444,282).

Sambonsugi teaches (at Figs 1A-1O; paragraphs 30-50) a method for forming a semiconductor device as applied to claims 1-6,11-16 and 20 above.

Re claims 7 and 17, Sambonsugi lacks mentioning a silicon-on-insulator substrate. Re claim 18, Sambonsugi lacks mentioning further steps for forming an interconnect in a contact opening formed in a dielectric.

However, Yamaguchi teaches (at Figs 1A-1B,2; col 1, line 25 through col 2) forming a semiconductor device on a silicon-on-insulator substrate (SOI; Fig 1B; col 1, lines 43-62) instead of on a bulk semiconductor substrate (Fig 1A; col 1, lines 23-42). Yamaguchi also teaches forming a dielectric over the gate 20 and the second junction region 17; forming a contact opening through the dielectric; and forming an interconnect 24 in the contact opening, the interconnect being electrically coupled to the junction region 17 (Fig 2; col 2, lines 13-21; Fig 5-6; col 5, line 35 through col 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor device of Sambonsugi on a silicon-on-insulator substrate as taught by Yamaguchi. This is because of the desirability to prevent soft error and latch up phenomenon, and to reduce device size. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to complete the method of forming the semiconductor device of Sambonsugi by forming an interconnect in a contact opening formed in a dielectric, as taught by Yamaguchi. This is because of the desirability to provide an electrical connection from the junction regions of the semiconductor device to an external terminal.

6. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sambonsugi et al (2003/0098486) taken with Akrams et al (5,719,425).

Sambonsugi teaches (at Figs 1A-1O; paragraphs 30-50) a method for forming a semiconductor device as applied to claims 1-6,11-16, and 20 above.

Re claims 8-10, Sambonsugi already teaches implanting dopants into the substrate by using the dopant dose of 1×10^{15} cm^{-2} for region 8N (para. 32); a dose of 7×10^{15} cm^{-2} for region 20 (para 38); and a dose 2×10^{15} cm^{-2} for region 31N (para 44). Sambonsugi thus just lacks mentioning the doping of the regions in a range of dopant concentrations (as in claims 8-10).

However, Akram et al teach (at col 6, lines 54-65; Figs 1A-1D) implanting impurities into the substrate to form the regions, wherein the dosages of 5×10^{13} to 5×10^{15} cm^{-2} would roughly correspond to the dopant concentrations from the range of 1×10^{17} cm^{3} to 1×10^{20} cm^{3} .

Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to implant impurities into the substrate to form the regions of Sambonsugi by selecting a portion of the prior art's range of dopant concentrations as taught by Akrams, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, see In re Aller, etal., 105 USPQ 233; In re Waite 77 USPQ 586 (CCPA 1948); In Re Swanson 56 USPQ 372 (CCPA 1942), wherein lightly doped regions at least reduce hot carrier effect, peak value, and overlap capacitance.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sambonsugi et al (2003/0098486) taken with Wang et al (6,713,357).

Sambonsugi teaches (at Figs 1A-1O; paragraphs 30-50) a method for forming a semiconductor device as applied to claims 1-6,11-16, and 20 above.

Re claim 19, Sambonsugi already teaches removing the first spacer, but lacks mentioning an etch step using hot H_3PO_4 acid.

However, Wang teaches (at col 7, lines 15-25; Figs 1E-1F) removing the first spacer 12 by performing an etch step using hot using hot phosphoric acid (H_3PO_4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to removing the first spacer of Sambonsugi by performing an etch step using hot using hot phosphoric acid (H_3PO_4) as taught by Wang. This is because the hot phosphoric acid is an effective chemical solution for etching to selectively remove the first spacer from the substrate.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-01

Michael Trinh
Primary Examiner